2. The messaging mechanism of claim 1, wherein the line processor receiving the system management interrupt will access the command delivered to [a] the respective mailbox, interpret the command and deliver [the] an appropriate response to [the] a mailbox.

5. The messaging mechanism of claim 1 wherein the at least one line processor is operable to conserve backplane bandwidth by selectively consolidating selected tasks onto the service processor to reduce the number of accesses to [the] a backplane to which the service processor and the at least one line processor are coupled.

6. A method for inter-processor communication messaging comprising the steps of:
providing a shared processor serving as a single point of contact for a user interfacing with at least one line processor,

providing mailboxes for each of the at least one line processors [at] and the shared processor enabling communication between the at least one line processor and the shared processor;

selectively delivering commands from the shared processor to a respective mailbox of a selected one of said at least one line processor, and

selectively issuing a system management interrupt from the shared processor to any or all of the at least one line processors, the interrupt signal[l]ing to the at least one line processor to access a respective mailbox in the shared memory.

7. The messaging method of claim 6, further comprising the step of:
causing the at least one line processor to access, in response to a system management interrupt, [a] the respective mailbox, interpret the command and deliver the appropriate response to a mailbox.

8. The messaging mechanism of claim 7, further comprising the step of:
[delivering a reponse to the respective mailbox;]

causing the at least one line processor to assert its system management interrupt line to the shared processor to indicate that said response has been delivered.